EAST SEARCH

11/10/03

L#	Hits	Search String	Databases
L2	751	integrated circuit with "analog circuit"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	435	integrated circuit with "mixed signal"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	3188	integrated circuit with (RF or "radio frequency")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	4251	("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integrat	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	0	(("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integra	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	0	(("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integra	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	97	(("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integra	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	49	(("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integrated circuit" with (RF or "radio frequency"))) and ((test$3 or verify or verification) with "digital circuit")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	119	(((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integrated circuit" with (RF or "radio frequency"))) and ((emulation or test$3 or verify or verification) with ("analog circuit" or "digital circuit" or FPGA))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	0	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	1645	(("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integra	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	21	(("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integra	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	45	((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integr	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	35	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	23	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L8	6	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	5	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	7	((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integr	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	31	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	9	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	1	(("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integra	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	2	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L1	0	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	3	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	13	((((("integrated circuit" with "analog circuit") or ("integrated circuit" with "mixed signal") or ("integ	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L1	2	6,272,465.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	1	1 and ("analog circuit" or "mixed signal" or RF or "radio frequency")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	1	2 and emulation and ("logic block" or "control block")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	1	3 and noise and "configuration register" and decoder	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	751	integrated circuit with "analog circuit"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	14	("integrated circuit" with "analog circuit") and emulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

	378	analog circuit and emulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	22	("analog circuit" and emulat$3) and "mixed signal"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	408	(test$3 or verify or verification) with "analog circuit"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	19	emulat$3 with "analog circuit"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	33	emulat$3 same "analog circuit"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	438	((test$3 or verify or verification) with "analog circuit") or (emulat$3 same "analog circuit")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	2	(((test$3 or verify or verification) with "analog circuit") or (emulat$3 same "analog circuit")) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	10	(((test$3 or verify or verification) with "analog circuit") or (emulat$3 same "analog circuit")) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	2	analog circuit same (array with "shift register")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	1	analog circuit same (("logic block" or "logic cell" or module) with "shift register")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	3662	circuit and (array with "shift register")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	82	analog circuit and (array with "shift register")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	3	("analog circuit" and (array with "shift register")) and emulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	136	digital circuit and (array with "shift register")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	20	("digital circuit" and (array with "shift register")) and emulat$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	149	(((test$3 or verify or verification) with "analog circuit") or (emulat$3 same "analog circuit")) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	50	(((test$3 or verify or verification) with "analog circuit") or (emulat$3 same "analog circuit")) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	0	(((test$3 or verify or verification) with "analog circuit") or (emulat$3 same "analog circuit")) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	39	(((test$3 or verify or verification) with "analog circuit") or (emulat$3 same "analog circuit")) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	22	(((test$3 or verify or verification) with "analog circuit") or (emulat$3 same "analog circuit")) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	1	(((test$3 or verify or verification) with "analog circuit") or (emulat$3 same "analog circuit")) and	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L1	8	"analog circuit" and (flip-flop$1 with pad$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	1	6,625,557.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	1	2 and "analog circuit" and "RF circuit"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	2	5,668,507.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	1	5 and (noise with "digital circuit")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	1321	"analog circuit" and (noise with generat$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L8	31	7 and ("digital circuit" with gate$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	12	6,460,172.pn. or 5,668,507.pn. or 6,389,567.pn. or 5,193,070.pn. or 6,005,407.pn. or 5,563,52	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	3	5,107,208.pn. or 6,625,557.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	15	9 or 10	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	7	11 and (control with (block$1 or cell$1 or logic))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	3392	"analog circuit" and (control with (block$1 or cell$1 or logic))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L14	153	13 and ((control with (block$1 or cell$1 or logic)) with configuration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L15	37	14 and (configuration with register$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L16	15	15 and (configuration same decoder$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L17	0	15 and (configuration with ("Exclusive OR" or Exclusive-OR or EXOR))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L18	0	14 and (configuration with ("Exclusive OR" or Exclusive-OR or EXOR))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L19	2	13 and (configuration with ("Exclusive OR" or Exclusive-OR or EXOR))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L20	0	"analog circuit" and (configuration with register$1 with ("Exclusive OR" or Exclusive-OR or EX	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L21	3	"digital circuit" and (configuration with register$1 with ("Exclusive OR" or Exclusive-OR or EX(	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

EAST SEARCH

11/10/03

Results of search set L10:("integrated circuit" with ("analog circuit" or "mixed signal" or RF or "radio frequency")) and emulation

Document	Kind Codes	Title	Issue Date	Current OR	Abstract
US 20020194560	A1	Method of and apparatus for testing a serial differential/mixed signal device	20021219	12	714/724
US 20020157050	A1	Position independent testing of circuits	20021024	51	714/726
US 20020147950	A1	Method and apparatus for test connectivity, communication, and control	20021010	42	714/726
US 20020041242	A1	Semiconductor apparatus	20020411	45	341/120
US 20010055281	A1	Software modem architecture	20011227	16	370/280
US 6571106	B1	Method and apparatus for glitchless signal generation	20030527	12	
US 6560734	B1	IC with addressable test port	20030506	51	714/724
US 6460172	B1	Microprocessor based mixed signal field programmable integrated device and prototyping meth	20021001	8	716/17
US 6405335	B1	Position independent testing of circuits	20020611	49	714/726
US 6378093	B1	Controller for scan distributor and controller architecture	20020423	40	714/726
US 6339388	B1	Mixed analog and digital integrated circuit and testing method thereof	20020115	12	341/120
US 6272465	B1	Monolithic PC audio circuit	20010807	230	704/258
US 6104217	A	Power on/off control circuit and method	20000815	16	327/111
US 5826093	A	Dual function disk drive integrated circuit for master mode and slave mode operations	19981020	35	712/43
US 5745777	A	Analyzer for frequency modulated signals	19980428	26	375/228
US 5638405	A	Dual-mode baseband controller for radio-frequency interfaces relating to digital cordless teleph	19970610	12	375/298
US 5526365	A	Method and apparatus for streamlined testing of electrical circuits	19960611	42	714/726
US 5457802	A	Integrated circuit pin control apparatus and method thereof in a data processing system	19951010	15	713/320
US 5163161	A	Fast scanning radio receiver with frequency data base management by remote processor	19921110	47	455/164.1
US 4931748	A	Integrated circuit with clock generator	19900605	14	331/1A
US 6460172	B	Microprocessor-based mixed-signal field programmable integrated circuit for integrated coin re	20021001	8	

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1. **Mentor Graphics Announces Scalable Verification Platform; New Technologies Help Bridge the Verification Gap**
   Business Editors. **Business Wire.** New York: Oct 27, 2003. p. 1
   Full text | Abstract

2. **Tuned up: 30th annual Microprocessor Directory**
   Robert Cravotta. **EDN.** Boston: Sep 4, 2003. Vol. 48, Iss. 19; p. 45
   Text+Graphics | Page Image - PDF | Citation

3. **Accellera Approves Four New Design Verification Standards**
   Business Editors/High-Tech Writers. **Business Wire.** New York: Jun 2, 2003. p. 1
   Full text | Abstract

4. **CADENCE DESIGN SYSTEMS: New Cadence Incisive verification platform compresses overall verification of nanometer-scale designs by up to 50 percent; Platform is first single-kernel solution with acceleration-on-demand**
   M2 Presswire. Coventry: Feb 24, 2003. p. 1
   Full text | Abstract

5. **Get a high-level view of wireless design**
   John Blyler. **Wireless Systems Design.** Cleveland: Feb 2002. Vol. 7, Iss. 2; p. 21 (4 pages)
   Text+Graphics | Page Image - PDF | Abstract

6. **TI's Mixed Signal Flash MCU Delivers the World's Lowest Power SoC Solution for Embedded Display Applications**
   PR Newswire. New York: Jan 22, 2002. p. 1
   Full text | Abstract

7. **Tools for embedded developers**
   Anonymous. **Embedded Systems Programming.** San Francisco: Dec 2001. Vol. 14, Iss. 13; p. 70 (4 pages)
   Text+Graphics | Page Image - PDF | Abstract

8. **FPGAs offer one-tenth the gates of ASICs**
   Pete Gasperini. **Electronic N ws.** New York: Sep 3, 2001. Vol. 47, Iss. 36; p. 16 (1 page)
   Full text | Page Image - PDF | Abstract

9. **Xicor Adds LabVIEW Tool Support for Mixed Signal Product Family; LabVIEW Supports High-Volume Device Programming for Manufacturing Applications**
   Business Editors/High-Tech Writers. **Business Wire.** New York: Nov 20, 2000. p. 1

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10. **Cygnal SoC pushes 8051 speed**
David Lammers. **Electronic Engineering Times.** Manhasset: Aug 7, 2000. p. 20 (1 page)
Text+Graphics Page Image - PDF Citation

11. **Texas Instruments Announces Next Generation GoldenPort(TM) RAS 'Universal Port' Solution Delivering Lowest Power and Highest Density Per Port with Market Leading Voice, Fax and Modem over IP Software; Complete Integrated Solution Based on TMS320C5440(TM), Newest Member of TI's TMS320C5000(TM) DSP Platform**
PR Newswire. New York: Mar 27, 2000. p. 1
Full text Abstract

12. **Texas Instruments Introduces Highest Performance DSP Solution For Digital Control Systems**
PR Newswire. New York: Mar 20, 2000. p. 1
Full text Abstract

13. **B.O.S. - Better On-line Solutions Affiliate Surf Software Helps Deliver Market-Leading Channel Densities For Texas Instruments' New C64x DSPs**
Business & Technology Editors. **Business Wire.** New York: Feb 25, 2000. p. 1
Full text Abstract

14. **Two Programmable TI DSPs Slash Power-per-Channel in Half for Integrated Voice, Fax and Data Over the Internet**
PR Newswire. New York: Dec 13, 1999. p. 1
Full text Abstract

15. **Agfa Universal Font Scaling Technology Integrated into Texas Instruments xStream DSP Technology For Color Laser Printers**
Business/Technology Editors. **Business Wire.** New York: Nov 17, 1999. p. 1
Full text Abstract

16. **Texas Instruments Drives Toward Sub 1-Volt Power With Delivery of the Industry's First 1.2-Volt DSP**
PR Newswire. New York: May 4, 1999. p. 1
Full text Abstract

17. **Looking ahead at new products**
Carol Rosen. **ECN.** Radnor: Jan 1999. Vol. 43, Iss. 1; p. 31 (2 pages)
Text+Graphics Page Image - PDF Abstract

18. **Design software**
Ann Steffora. **Electronic News.** New York: Aug 24, 1998. Vol. 44, Iss. 2233; p. 33 (1 page)
Full text Page Image - PDF Citation

19. **Mentor Graphics Reports Six-Percent Revenue Growth for the 1998 First Quarter**
PR Newswire. New York: Apr 30, 1998. p. 1
Full text Abstract

20. **Mobile chips: Towards a common platform**
Anil Aggarwal. **Telecommunications International.** Norwood: Apr 1998. Vol. 32, Iss. 4; p. 86 (3 pages)
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21. **NATIONAL SEMICONDUCTOR: Industry's most integrated silicon solutions for DECT cordless phon s announced**
M2 Presswire. Coventry: Jan 28, 1998. p. 1

Full text Abstract

22. **Time to buy?**
Eric J Savitz. **Barron's.** Chicopee: Nov 10, 1997. Vol. 77, Iss. 45; p. 37 (11 pages)
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23. **The test floor**
Gale Bradley, Judy Erkanat. **Electronic News.** New York: Mar 10, 1997. Vol. 43, Iss. 2158; p. 46 (1 page)
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24. **Analog Devices enhances GSM handset solution**
Gutcho, Lynette. **PR Newswire.** New York: Nov 11, 1996. p. 1 (1 page)
Full text Abstract

25. **ATM, Sonet Chip Markets Set To Take Off**
Bill Arnold. **EBN.** Manhasset: Oct 23, 1995. p. 24
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Computer - Aided Engineering. Cleveland: Nov 1993. Vol. 12, Iss. 11; p. 36 (4 pages)
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1 Optimized implementations of the multi-configuration DFT technique for analog circuits 88%
M. Renovell , F. Azaïs , Y. Bertrand
Proceedings of the conference on Design, automation and test in Europe February 1998
The paper describes an approach to optimize the application of the multi-configuration DFT technique for analog circuits. This technique allows to emulate the circuit in a number of new test configurations targeting the maximum fault coverage. The brute force application of the multi-configuration is shown to produce a very significant improvement of the original poor testability. An optimized approach is proposed to apply this DFT technique in a more refined way. The optimization problem consis ...

2 Built-In Dynamic Current Sensor for Hard-to-Detect Faults in Mixed-Signal Ics 82%
Y. Lechuga , R. Mozuelos , M. Martínez , S. Bracho
Proceedings of the conference on Design, automation and test in Europe March 2002
There are some types of faults in analogue and mixedsignal circuits which are very difficult to detect usingeither voltage or current based test methods. However, itis possible to detect these faults if we add to theconventional dynamic power supply current test methodsIDDT, the analysis of the changes in the slope of thisdynamic power supply current. In this work, we present aBuilt-In Current Sensor (BICS) which is able to processthe highest frequency components in the dynamic powersupply curre ...

3 System level modeling and verification: Embedded systems verification with FGPA-enhanced in-circuit emulator 80%
M. Meerwein , C. Baumgartner , T. Wieja , W. Glauert
Proceedings of the 13th international symposium on System synthesis September 2000
In this paper we present a novel coverification concept for embedded microcontrollers that satisfies industrial requirements. Based on a commercially available CPU in-circuit emulator coupled with FPGA boards, it verifies the correctness of an implementation in terms of function and timing within a real-world environment.Using our system, the software engineer can write, test and optimize programs for a chip that is not yet physically existent. In addition the system is used to obtain software m ...

4 Metrics, techniques and recent developments in mixed-signal testing 80%
Gordon W. Roberts
Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997
This paper presents a tutorial on mixed-signal testing. Our focus is on testing the analog portion of the mixed-signal device, as the digital portion is handled in the usual way. We begin by first outlining the role of test in a manufacturing environment, and its impact on product cost and quality. We look at the impact of manufacturing defects on the behavior of digital and analog circuits. Subsequently, we argue that analog circuits require very different test methods than those presently used ...

5 A Functional Specification Notation for Co-Design of Mixed Analog-Digital Systems 77%
A. Dobol , R. Vemuri
Proceedings of the conference on Design, automation and test in Europe March 2002
This paper discusses aBlox - a specification notation forhigh-level synthesis of mixed-signal systems. aBlox addressesthree important aspects of mixed-signal system specification:(1) description of functionality and (2) performanceissues and (3) expression of analog-digital interactions.The semantics of aBlox embeds concepts and rulesof a functional computational model, and uses a declarativestyle to denote performance elements. The papershows some mixed-signal specifications that we developedin ...

6 Mixed-signal design and simulation: Characterizing the effects of clock jitter due to substrate noise in discrete-time D/S modulators 77%
Payam Heydari
Proceedings of the 40th conference on Design automation June 2003
This paper investigates the impact of clock jitter induced by substrate noise on the performance of the oversampling DS modulators. First, a new stochastic model for substrate noise is proposed. This model is then utilized to study the clock jitter in clock generators incorporating phase-locked loops (PLLs). Next, the effect of the clock jitter on the performance of the DS modulator is studied. It will be shown that substrate noise degrades the signal-to-noise ratio of the DS modulator while the ...

7 Session 1: multimedia networking: Multi-party distributed audio service with TCP fairness 77%
Milena Radenkovic , Chris Greenhalgh
Proceedings of the tenth ACM international conference on Multimedia December 2002
Distributed Partial Mixing is an approach to creating a distributed audio service that supports optimisation of bandwidth utilization across multiple related audio streams (e.g. from concurrently active audio sources) while maintaining fairness to TCP traffic in best effort networks. Rate adaptation of streamed audio is difficult because of its rate sensitivity, the relatively limited range of encoding bandwidths available and the potential impact on the end user of rate-adaptation artefacts (su ...

8 Energy-aware design of embedded memories: A survey of technologies, architectures, and optimization techniques 77%
Luca Benini , Alberto Macii , Massimo Poncino
ACM Transactions on Embedded Computing Systems (TECS) February 2003
Volume 2 Issue 1

Embedded systems are often designed under stringent energy consumption budgets, to limit heat generation and battery size. Since memory systems consume a significant amount of energy to store and to forward data, it is then imperative to balance power consumption and performance in memory system design. Contemporary system design focuses on the trade-off between performance and energy consumption in processing and storage units, as well as in their interconnections. Although memory design is as ...

9 Poster Session 3: Dynamic Vt SRAM: a leakage tolerant cache memory for low voltage microprocessors 77%

Chris H. Kim , Kaushik Roy

Proceedings of the 2002 international symposium on Low power electronics and design August 2002

This paper presents a Dynamic V_t SRAM (DTSRAM) architecture to reduce the subthreshold leakage in cache memories. The V_t of each cache line is controlled separately by means of body biasing. In order to minimize the energy and delay overhead, a cache line is switched to high V_t only when it is not likely to be accessed anymore. Simulation results from SimpleScalar framework show that even after considering the energy overhead, the DTSRAM can save 72% of the cache ...

10 Intrinsic response for analog module testing using an analog testability bus 77%

Chauchin Su , Yue-Tsang Chen , Shyh-Jye Jou

ACM Transactions on Design Automation of Electronic Systems (TODAES) April 2001 Volume 6 Issue 2

A parasitic effect removal methodology is proposed to handle the large parasitic effects in analog testability buses. The removal is done by an on-chip test generation technique and an intrinsic response extraction algorithm. On-chip test generation creates test signals on-chip to avoid the parasitic effects of the test application bus. The intrinsic response extraction cross-checks and cancels the parasitic effects of both test application and response observation paths. The tests using bo ...

11 Integrated high-level synthesis and power-net routing for digital design under switching noise constraints 77%

Alex Doboli , Ranga Vemuri

Proceedings of the 38th conference on Design automation June 2001

This paper presents a CAD methodology and a tool for high-level synthesis (HLS) of digital hardware for mixed analog-digital chips. In contrast to HLS for digital applications, HLS for mixed-signal systems is mainly challenged by constraints, such as digital switching noise (DSN), that are due to the analog circuits. This paper discusses an integrated approach to HLS and power net routing for effectively reducing DSN. Motivation for this research is that HLS has a high impact on DSN reducti ...

12 An overview of the Georgia Tech Broadband Institute at the Georgia Institute of Technology, Atlanta, USA 77%

Nikil Jayant , John Pippin

ACM SIGMOBILE Mobile Computing and Communications Review April 2000 Volume 4 Issue 2

The Georgia Tech Broadband Institute was created in 1999, as a combination of two evolving

organizations --- the Broadband Telecommunications Center (created in 1995) and the Georgia Tech Wireless Institute (created in 1998). The consolidation of the centers was in reflection of the synergy that existed between the centers, and the overlap in terms of existing and potential Industry sponsorship. The 1999 merger recognized that the future of wireless included an overarching trend towards broadban ...

13 What is the proper system on chip design methodology (panel) 77%
Richard Goering , Pierre Bricaud , James G. Dougherty , Steve Glaser , Michael Keating , Robert Payne , Davoud Samani
Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

14 Metrology for analog module testing using analog testability bus 77%
Chauchin Su , Yue-Tsang Chen , Shyh-Jye Jou , Yuan-Tzu Ting
Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997
In this paper, we propose a method to generate high quality test waveform on chip to avoid the parasitic effects in an analog testability bus test environment. For the test response analysis, we derive an extraction methodology to remove the parasitic effects and obtain the intrinsic response of the CUT. The test results show that the algorithm is robust such that the intrinsic responses remain the same regardless of the small variation in the test waveforms. With the concept of intrinsic respon ...

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